ABSTRACT

An IC fabrication method comprises the steps of: providing a substrate (10, 41); forming an active region (41) for a bipolar transistor and an active region (41) for a MOS device in the substrate (10); forming isolation areas (81) around, in a horizontal plane, the active regions; forming a MOS gate region (111, 112) on the active region for the MOS device; forming a layer (141) of an insulating material on the MOS gate region and on the active region (31) for the transistor; and defining a base region in the active region for the transistor by producing an opening (143) in the insulating layer (141) such that the remaining portions of the insulating layer (141) partly cover the active region for the bipolar transistor. The insulating layer (141) remains on the MOS gate region to encapsulate and protect the MOS gate region during subsequent manufacturing steps.